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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,474	02/20/2004	Jian-Shen Yu	B-5381 621721-5	7461

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EXAMINER	
SHERMAN, STEPHEN G	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,474	YU ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-7* is/are rejected.

7)☒ Claim(s) *4 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 5 is objected to because of the following informalities: The second line of claim 5 states: "a plurality of display units, arranged in array." The line should be changed to state: "a plurality of display units, arranged in **an** array.". Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3 and 5-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Higashi (US 6,023,260).

Regarding claim 1, Higashi discloses a sampling circuit (Figure 3, circuit 261) for an analog signal according to a clock signal, comprising:

a first thin film transistor (TFT) (Figure 3, transistor 410),

having a first electrode to receive the analog signal (Figure 3 shows that transistor 410 receives on a first electrode analog signal S1 as explained in column 7, lines 7-10.),

a control electrode to receive the clock signal (Figure 3 shows that the control electrode of transistor 410 is connected to the clock signal output 240.) and

a second electrode for sampling the analog signal when the clock signal is at a first logic level (Figure 3 shows that transistor 410 has a second electrode for sampling the analog signal when the clock signal turns the transistor on/off.); and

a counteracting device (Figure 3, capacitor 412.) coupled to the second electrode (Figure 3 shows that capacitor 412 is coupled to the second electrode of transistor 410.),

wherein when the clock signal is changed from the first logic level to a second logic level, feed-through voltage drop caused by a parasitic capacitance between the second electrode and the control electrode of the first TFT is reduced (The examiner understands that since the structure of Higashi is the same as the structure in the specification, the circuit of Higashi will inherently reduce the feed-through voltage drop caused by a parasitic capacitance when the transistor 410 is turned on/off by the clock signal.).

Regarding claim 2, Higashi discloses the circuit as claimed in claim 1, wherein the counteracting device is a capacitor between the second electrode and a reference potential node (Figure 3 shows capacitor 412 which I coupled between the second

electrode and ground.).

Regarding claim 3, Higashi discloses the circuit as claimed in claim 1, wherein the counteracting device comprises an inversion device, having an input terminal coupled to the control electrode, and a capacitor between the second electrode and a output terminal of the inversion device (Column 7, lines 34-38 explain that the analog switch of Figure 25A could be used in Figure 3. Figure 25a shows an inversion device, having an input terminal coupled to the control electrode of TFT 414 and then a transistor coupled between the second electrode and an output terminal of the inverter. Since in the specification it states that a transistor can be a capacitor, the transistor of Figure 25A could be a capacitor.).

Regarding claim 5, Higashi discloses a liquid crystal display (Figure 3), comprising:

a plurality of display units, arranged in array (Figures 1A and 1B and column 4, lines 47-64.);

a plurality of data lines disposed corresponding to each line of the display units, wherein each data line provides a video signal to the corresponding display unit (Figure 3 D(1)-D(k) and column 7, lines 7-10.); and

a data driving circuit (Figure 1A, item 200 and column 4, lines 65-67.), having at least one sampling circuit, sampling an image signal to be the video signal according to a clock signal (Figure 3, circuit 261), and the sampling circuit comprising:

a first thin film transistor (TFT) (Figure 3, transistor 410),

having a first electrode to receive the analog signal (Figure 3 shows that transistor 410 receives on a first electrode analog signal S1 as explained in column 7, lines 7-10.),

a control electrode to receive the clock signal (Figure 3 shows that the control electrode of transistor 410 is connected to the clock signal output 240.) and

a second electrode for sampling the analog signal when the clock signal is at a first logic level (Figure 3 shows that transistor 410 has a second electrode for sampling the analog signal when the clock signal turns the transistor on/off.); and

a counteracting device (Figure 3, capacitor 412.) coupled to the second electrode (Figure 3 shows that capacitor 412 is coupled to the second electrode of transistor 410.),

wherein when the clock signal is changed from the first logic level to a second logic level, feed-through voltage drop caused by a parasitic capacitance between the second electrode and the control electrode of the first TFT is reduced (The examiner understands that since the structure of Higashi is the same as the structure in the specification, the circuit of Higashi will inherently reduce the feed-through voltage drop caused by a parasitic capacitance when the transistor 410 is turned on/off by the clock signal.).

Regarding claim 6, this claim is rejected under the same rationale as claim 2.

Regarding claim 7, this claim is rejected under the same rationale as claim 3.

Allowable Subject Matter

4. Claims 4 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter:

The primary reason for indicating allowable subject matter is that both claims 4 and 8 recite the limitation: " wherein the capacitor comprises a second TFT having a gate terminal coupled to the output terminal of the inversion device and a source and drain terminal both coupled to the second electrode," which is not found singularly or in combination within the prior art.

The closest prior art reference is Higashi (US 6,023,260) which teaches an inversion device with a transistor between the second electrode and an output terminal of the inversion device, however, Higashi fails to teach that the both the source and drain are coupled to the second electrode.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ozawa (US 6,864,874), Shimada et al. (US 5,801,673), Murakami et al. (US 6,392,629) and Zhang et al. (US 6,806,862) all teach of a sampling circuit in which a capacitor is coupled to an electrode of a TFT.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

14 March 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER